Lecture No 2

The Machine: Interpretation & Microprogramming

The Machine: Interpretation & Microprogramming

Management of *Interpretation* Process is responsibility of decoder.

The *Interpretation Process* begins with the decoding of opcode field from the *Instruction*.

OP Code field being decoded by the *Decoder*.

The Instruction

The *Decoder* activates *Registers* for a series of state transitions that correspond to the action of OP Code.

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The *Registers* used in *Instructions* can be both

Explicit* and *Implicit.

Explicit Registers Include:

- **General Purpose Registers (GPR)**
- **Accumulators (ACC)**
- **Address Registers (Index or Base Registers).**

The Machine: Interpretation & Microprogramming

The *Registers* used in *Instructions* can be both

Explicit* and *Implicit.

Implicit Registers Include:

- **PC (Program Counter) :**
  Contains address of next instruction in sequence.

- **Instruction Register :**
  This register holds the Instruction being interpreted or executed.

- **Memory Address Register (MAR)-**
  Contents of this register are used as address to locate information in the memory.

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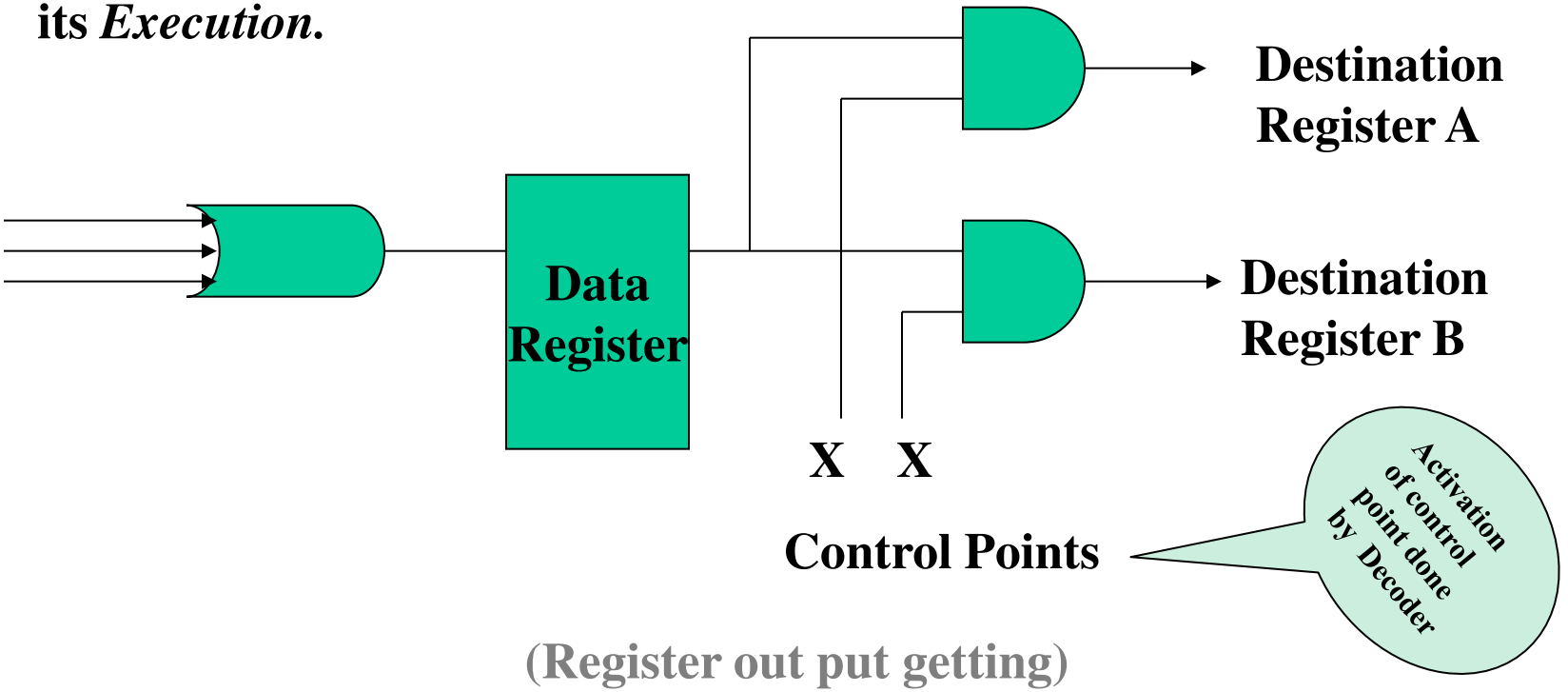
Decoder **controls the** ***Data Paths*** **consisting of combinational logic.**

What is Data Path ?

"Data path connect the output of one register to another register."

Each OP Code defines which of the various *data paths* will be used in its *Execution*.



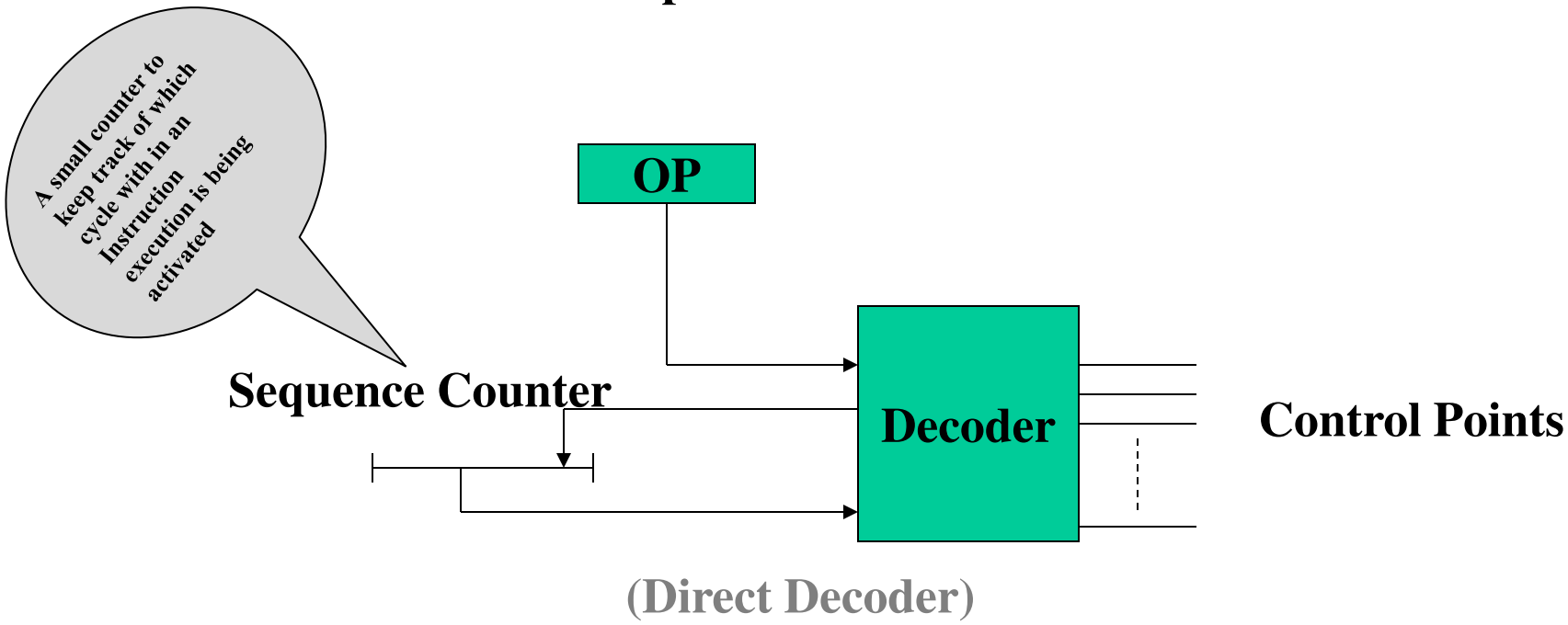
(Register out put getting)

The Machine: Interpretation & Microprogramming

Decoder **that manage interpretation is Direct or Microprogrammed Decoder**

1. ***Direct Decoder:***

   Direct Decoders are designed using combinational logic to represent the various desired control point actions.

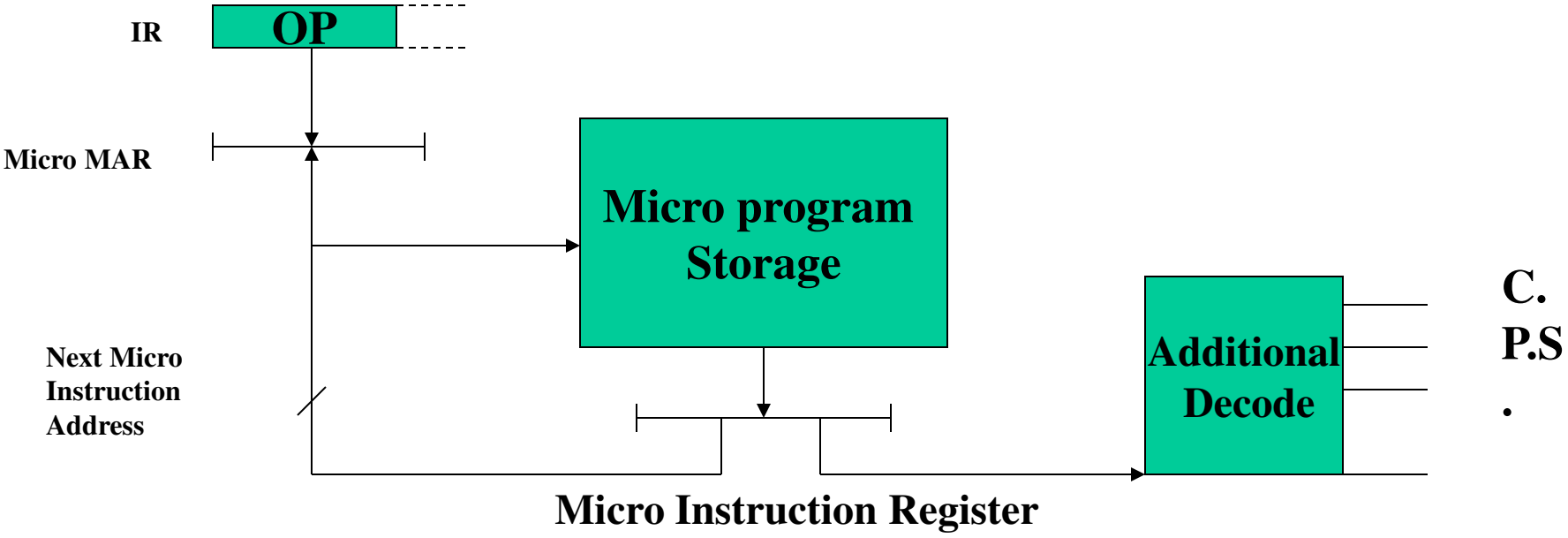


(Direct Decoder)

The Machine: Interpretation & Microprogramming

Decoder **that manage interpretation is Direct or Microprogrammed Decoder**

2. ***Microprogrammed Decoder:*** **are designed using ROM. The OP Code provides an initial address to an entry which specifies the control point values as well as the address of the next micro instruction.**



Direct Decoders Vs Micro programmed Decoders

Attribute	Direct Decoders	Micro Programmed Decoder
Speed	Fast	Slower
Chip Area Efficiency	Uses Least area	Uses More Area
Ease Of Change	Somewhat Difficult	Easier
Large/Complex Instruction Sets	Somewhat Difficult	Easier
Support of Operating Systems and Diagnostic Features	Very Difficult	Easy
Where Used	Mostly RISC M/C	Main Frames / Microprocessors
Instruction set size	Usually under 100	Usually over 100